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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 has been amended as follows:

1.(Amended) A method of manufacturing a semiconductor device, comprising the steps of:

[providing a semiconductor substrate in which a cell region and a peripheral circuit region are defined;]

forming a patterned tunnel oxide film, a floating gate electrode <u>a dielectric film</u>, and a control gate electrode in <u>said</u> <u>a</u> cell region <u>forming a gate electrode in said</u> <u>peripheral circuit region</u>] <u>of a semiconductor substrate;</u>

forming a gate electrode in [said] \underline{a} peripheral circuit region $\underline{of the}$

semiconductor substrate;

removing an exposed portion of a device isolation film in [said] the cell region by [means of] a [self align] self-align source etch process;

forming a first capping layer and a second capping layer on the [entire structure] semiconductor substrate;

performing a [self align] self-align source annealing process for [said] the cell region;

forming a source and drain junction in [said] the cell region [and];

forming a low concentration source and drain junction in [said] the peripheral circuit region;

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forming a gate spacer in [said] the peripheral circuit region; and forming a high concentration source and drain junction in [said] the peripheral circuit region.

Claim 2 has been amended as follows:

2.(Amended) The method [of manufacturing a semiconductor device] according to claim 1, wherein [said first capping layer is formed in thickness of 100 ~ 200 Å] <u>a</u> thickness of the first capping layer is 100-200Å.

Claim 3 has been amended as follows:

3.(Amended) The method [of manufacturing a semiconductor device] according to claim

1, wherein [said second capping layer is formed in thickness of 50 - 150 Å] a thickness of the second capping layer is 50-150Å.

Claim 4 has been amended as follows:

4.(Amended) The method [of manufacturing a semiconductor device] according to claim

1, wherein [said] the gate spacer is formed of [said] the first capping layer[/], [said] the

second capping layer[/], and an oxide film [for a spacer in a way that an oxide film for a

spacer is formed on said second capping layer and said oxide film for a spacer and said

second capping layer are then sequentially etched] by a blanket etch process.

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Claim 5 has been amended as follows:

5.(Amended) The method [of manufacturing a semiconductor device] according to claim

4, wherein [said oxide film for a spacer is formed in thickness of 1200 - 1600 Å] a

thickness of the oxide film is 1200-1600Å.

Claim 6 has been amended as follows:

6.(Amended) The method [of manufacturing a semiconductor device] according to claim

4, wherein [said] the oxide film [for a spacer] and [said] the first capping layer are etched

through [the mediation] to lateral portions of [said] the second capping layer to form a

screen oxide film.

Claim 7 has been amended as follows:

7.(Amended) The method [of manufacturing a semiconductor device] according to claim

1, wherein [said] the source and drain junction in [said] the cell region is formed by

using [said] the first capping layer and [said] the second capping layer as an ion

implantation screen oxide film.

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Claim 8 has been amended as follows:

8.(Amended) The method [of manufacturing a semiconductor device] according to claim

1, wherein [said] the low concentration source and drain junction in [said] the peripheral

circuit region is formed by using $\frac{\text{said}}{\text{the}}$ first capping layer and $\frac{\text{said}}{\text{the}}$ second

capping layer as an ion implantation screen oxide film.

Claim 9 has been amended as follows:

9.(Amended) The method [of manufacturing a semiconductor device] according to claim

1, wherein [said] the high concentration source and drain junction in [said] the peripheral

circuit region is formed by using a lateral portion of [said] the first capping layer etched

[by a given thickness] as an ion implantation screen oxide film.

Claim 10 has been amended as follows:

10.(Amended) The method [of manufacturing a semiconductor device] according to

claim 1, wherein [said] the first capping and [said] the second capping layer [functions

to] prohibit formation of a local bird's beak of [said] the dielectric film formed between

[said] the floating gate electrode and [said] the control gate electrode.